

## CLAIMS:

1. Method for operating an array (40) of non-volatile charge trapping memory devices (10), comprising:
  - before a block erase step (52) of substantially all of the non-volatile memory devices (10) of the array (40), block programming (51) of substantially all of the non-volatile memory devices (10) of the array (40).
2. Method according to claim 1, furthermore comprising after the erase operation (52), programming (53) some of the non-volatile memory devices (10) of the array (40), depending on data content to be stored in the non-volatile memory devices (10) of the array (40).
3. Method according to claim 2, furthermore comprising reading the data content stored in a non-volatile memory device (10) of the array (40), wherein for reading the data content stored in a non-volatile memory device (10) of the array (40) at least one further non-volatile memory device having a dielectric charge trapping layer is used as reference cell (45) which is programmed and erased for a block programming and block erase, respectively, of the non-volatile memory devices (10) in the array (40).
4. Method according to claim 3, wherein the memory devices (10) of the array (40) together function as reference cells.
5. An electrical device comprising an array of non-volatile charge trapping memory devices (10), comprising:
  - means for block programming (51) of substantially all of the non-volatile memory devices (10) of the array (40),
  - means for block erasing (52) of substantially all of the programmed non-volatile memory devices (10) of the array (40),
  - control means (73) for controlling the array of non-volatile memory devices (10) such that before block erasing of substantially all of the non-volatile memory devices of

the array, substantially all of the non-volatile memory devices of the array are block programmed.

6. An electrical device according to claim 5, wherein the non-volatile memory device (10) comprises a transistor having a channel and a control gate, a dielectric charge trapping layer (11) being located between the channel and the control gate.
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7. An electrical device according to claim 5, the array being provided with at least one non-volatile memory device (10) for use as a reference cell (45) in a sense amplifier.
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8. An electrical device according to claim 7, the array comprising means for programming and erasing the reference cell (45) for a block-programming and block-erasing respectively of the non-volatile memory devices (10) in the array (40).
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9. An electrical device according to claim 7, wherein the at least one reference cell (45) is separate from the array (40).
10. An electrical device according to claim 7, wherein the memory devices (10) of the array together function as reference cells.
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11. An electrical device according to claim 7, comprising means for comparing a read current from a non-volatile memory device (10) in the array (40) with a read current from the reference cell (45).
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12. An electrical device according to claim 7, comprising means for adapting a read current for reading the non-volatile memory devices (10) in the array (40) to the ageing of the reference cell (45).
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13. An electrical device according to claim 7, comprising means for adapting a required control gate voltage for reading the non-volatile memory devices (10) in the array (40), depending on the ageing of the reference cell (45).

14. An electrical device according to claim 5, wherein the array of non-volatile memory devices (10) forms a non-volatile memory.